In the Claims:

Please cancel claim 20. Please amend claims 15-16 and 21-25. Please add new claims 30-38. The claims are as follows:

1-14. (Canceled)

15. (Currently amended) A method of forming a semiconductor chip carrier, comprising the steps of:

providing a substrate, having a plated through hole therein;

forming a first power plane on a first external surface of the substrate and in direct mechanical contact with the first external surface;

forming a second power plane on a second external surface of the substrate and in direct mechanical contact with the second external surface;

depositing a first redistribution layer on [[a]] the first ~~and a second surface of the substrate~~ power plane and in direct mechanical contact with a surface of the first power plane, wherein the first power plane is disposed between the first redistribution layer and the first external surface; ~~and~~

depositing a second redistribution layer on the second power plane and in direct mechanical contact with the second power plane, wherein a surface of the second power plane is disposed between the second redistribution layer and the second external surface;

forming a first plated blind via within the first redistribution layer, wherein the first via is in ~~selectively positioned over and~~ electrically contacting with the plated through hole, and

wherein the first via is in direct mechanical and electrical contact with the first power plane; and

forming a second plated blind via in the second redistribution layer, wherein the second via is in electrical contact with the plated through hole, and wherein the second via is in direct mechanical and electrical contact with the second power plane.

16. (Currently amended) The method of claim 15, further including the step of:

forming a chip connection pad in the first via.

17. (Original) The method of claim 15, wherein the step of providing a substrate, having a plated through hole therein includes the steps of:

drilling a hole through the substrate;

cleaning the hole; and

forming a conductive layer on an interior surface of the hole.

18. (Original) The method of claim 15, further comprising the step of:

filling the plated through hole with a reinforcing material.

19. (Original) The method of claim 18, wherein the reinforcing material comprises an electrically conductive material.

20. (Canceled)

21. (Original) The method of claim 15, wherein the step of providing a substrate, having a plated through hole therein further includes the steps of:

providing a ground plane;

forming a first pair of signal planes within the substrate;

forming a first pair of power cores within the substrate;

forming a second pair of signal planes within the substrate; ~~and~~

~~forming a second pair of power cores within the substrate.~~

22. (Currently amended) ~~The method of claim 21~~ A method of forming a semiconductor chip carrier, comprising the steps of:

providing a substrate, having a plated through hole therein;

depositing a redistribution layer on a first and a second surface of the substrate; and

forming a via within the redistribution layer, selectively positioned over and electrically contacting the plated through hole, wherein the step of providing a substrate, having a plated through hole therein further includes the steps of:

providing a ground plane;

forming a first pair of signal planes within the substrate;

forming a first pair of power cores within the substrate;

forming a second pair of signal planes within the substrate; and

forming a second pair of power cores within the substrate, wherein the first and second pair of signal planes are controlled impedance circuitry.

23. (Currently amended) ~~The method of claim 21~~ A method of forming a semiconductor chip carrier, comprising the steps of:

providing a substrate, having a plated through hole therein;

depositing a redistribution layer on a first and a second surface of the substrate; and

forming a via within the redistribution layer, selectively positioned over and electrically contacting the plated through hole, wherein the step of providing a substrate, having a plated through hole therein further includes the steps of:

providing a ground plane;

forming a first pair of signal planes within the substrate;

forming a first pair of power cores within the substrate;

forming a second pair of signal planes within the substrate; and

forming a second pair of power cores within the substrate, wherein the second pair of power cores are directly underneath and electrically connected to portions of the redistribution layer.

24. (Currently amended) The method of claim ~~23~~ 15, wherein the first and second ~~pair of~~ power planes respectively ~~cores further~~ include[[s]] a top surface metallurgy (TSM) and a bottom surface metallurgy (BSM).

25. (Currently amended) The method of claim 15, wherein the first redistribution layer comprises a fatigue resistant dielectric material.

26. (Original) The method of claim 15, further comprising the step of:

providing a buried plated through hole in the substrate.

27-29. (Canceled)

30. (New) The method of claim 15, further comprising:

roughening the surface of the first power plane, thereby enhancing an adhesion of the first redistribution layer to the first power plane; and

roughening the surface of the second power plane, thereby enhancing an adhesion of the second redistribution layer to the second power plane.

31. (New) The method of claim 30, wherein the first and second power planes each comprises copper, and wherein roughening the surface of the first and second power planes comprises treating the surface of the first and second power planes with chlorite.

32. (New) The method of claim 15, wherein the first and second redistribution layers each comprise a dielectric material having a flexibility that reduces internal stresses resulting from thermal cycling of the substrate, the first and second power planes, and the first and second redistribution layers.

33. (New) The method of claim 15, further comprising:

forming a Controlled Collapse Chip Connection (C4) pad through the first redistribution

layer as part of and connected to the first via; and

forming a Ball Grid Array (BGA) pad directly on and connected to the second via.

34. (New) The method of claim 15, wherein the first via is in selectively aligned directly over the plated through hole.

35. (New) The method of claim 34, wherein the second via is aligned directly over the plated through hole.

36. (New) The method of claim 34, wherein the second via is offset from the plated through hole.

37. (New) The method of claim 15, wherein the first via is offset from the plated through hole.

38. (New) The method of claim 37, wherein the second via is offset from the plated through hole.